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PATENT

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PTO-1449 Information Disclosure Citation In an Application	Application No. 10/685,629	Applicant(s): WONG, ET AL.	
	Docket Number 068354.1180	Group Art Unit 2814	Filing Date October 15, 2003

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
LP	A	US 5,879,990	03.09.1999	DORMANS, ET AL.	438	257	03.11.1997
	B	US 6,251,728 B1	06.26.2001	PATELMO, ET AL.	438	257	07.22.1999
	C	US 5,956,584	09.21.1999	SHYE-LIN WU	438	232	03.30.1998
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FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
LP	D	EP 0 811 983 A1	10.12.1997	EUROPE	G11C 11	34	X	

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
LP	E	WONG, JACK AND DARYANANI, SONU, METHOD OF FORMING HIGH VOLTAGE CMOS TRANSISTORS USING A MODIFIED SADS PROCESS, MICROCHIP TECHNOLOGY, INC., TEMPE, AZ.	

Long Pham 3/28/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.